CLAIMS

**What is claimed is:**

1. A method for performing arithmetic in a memory to memory architecture in an embedded processor, the method comprising:

receiving a 32-bit fixed length instruction, the instruction specifying a source address in a memory using 11 bits, a source address in a register file using 5 bits, a destination address in the memory using 11 bits, and a mathematical operation to be performed using 5 bits; and

responsive to receiving the fixed length instruction:

accessing, from the source address in the memory, a first operand on which the mathematical operation is to be performed;

accessing, from the source address in the register file, a second operand on which the mathematical operation is to be performed;

performing the mathematical operation on the first operand and the second operand to obtain the result; and

storing the result in the destination address in the memory.